Optimization of SRAM Circuits for Dynamic Voltage Scalable Applications in 7nm FinFET Technology

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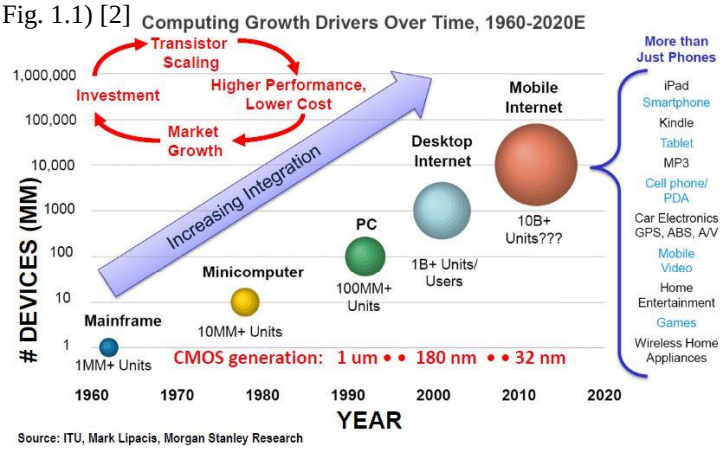
1.0 Introduction: Impact of Moore's Law and Ultra-Thin Body FinFETs

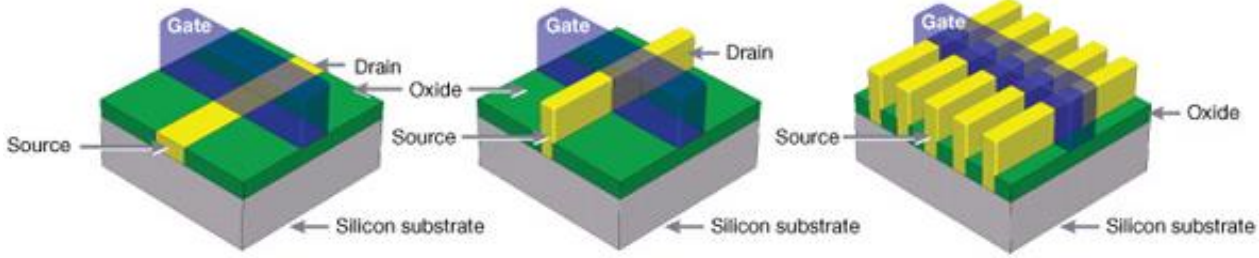
The digital revolution and the ever increasing computational power it has enabled have been driven by the continued scaling of semiconductor technologies in the form of CMOS transistors, constituent to integrated circuits (ICs) in modern-day microprocessor [1]. This scaling allows the transistor density to nearly double about every two years, in a phenomenon called Moore's Law. For the past four decades the advance of Moore's Law has brought about rapid changes to computer technology; enabling revolutionary innovations such as the Internet, personal laptop, and smart electronics. Measuring this scaling in terms of gate length of MOSFETs, the current gate length stands around L_g = 30nm [1].

Fig. 1.1) [2]



Recently, this phenomenal increase in transistor scaling has slowed. This is mainly due to difficulties arising from prohibitive device variations—affecting the parameters like the threshold voltage v_t—and detrimental short-channel effects [1]. In particular, random variations in v_t possesses a serious challenge for scaling SRAM cell area and operating voltage at 22nm and beyond [3]. The source of variation of v_t comes from both systematic and random variations. Lithography-induced variations in channel length and width are systematic which means that they are deterministic. Random sources originate from random dopant fluctuations (RDF), gate work-function variation (WFV), and line-edge-roughness (LER) [3]. To combat v_t fluctuations, designers have modified the old planar MOSFET structure on bulk silicon in attempt to enable continued scaling [1]. This had led to two main-candidates: planar fully-depleted (FD) SOI MOSFET, and the 3D (also FD) FinFET. Both of these structures rely on ultra-thin body (UTB) to help control the SCEs [1].

Fig. 1.2) Planar MOSFET, Single-Gated (SG) FinFET, and Multiple-Gated FinFET Structures [8]

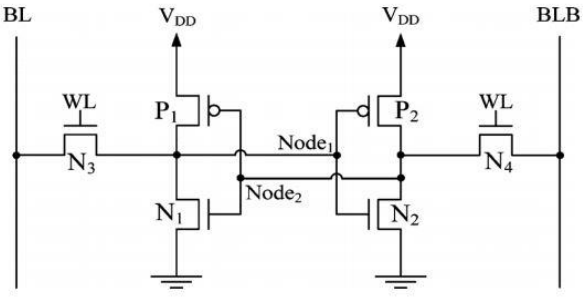


1.1 Static Random Access Memory: Device Operation and Characterization

Static random access memory (SRAM) is one form of VLSI device widely produced today. SRAM is defined as any device with two stable, electrical states that can be externally programmed [4]. Depending on the storage element, one or more access transistors are connected to an SRAM cell. Commercially produced SRAM storage constitutes an array of memory cells that be accessed individually.

Each SRAM cell is formed by a bistable latch of two cross-coupled CMOS inverters associated with two access transistors. The nodes 1 and 2 stores a single bit of memory at the intersection point of the two nodes transfer characteristics. When displayed visually they form a "butterfly" plot for the pair of cross-coupled inverters. Basic device operations include read and write. To read a single bit, the wordlines turned high allowing the logical state to be sensed via the bitlines. To write, appropriate signal voltages are applied to the bitlines (BL and BLB), forcing the nodes to re-settle into a new equilibrium along their butterfly curves [4].

Fig. 1.3) 6T-SRAM Cell Layout Schematic [5]



To characterize the effectiveness of SRAM cells, static noise margins (SNM) and write voltage margins (WVM) are extensively used, though other parameters are also used. Static noise margin is defined as the maximum noise voltage needed to cause a flip in stored logical state of an SRAM cell. It can be thought as the

maximum tolerance to external voltage disturbance before a change of state happens [5]. Graphically, the static noise margin is the measured by the side of the maximum square that can be nested between two transfer curves. In standby or hold mode, SRAM's butterfly transfer curve maintains the largest SNM values. However, during read access, the shifting of transfer characteristics significantly degrades the static noise margin. As such the read static noise margin (RSNM) is always less than the hold static noise margin (HSNM) [5].

Write voltage margin is defined as the difference between supply voltage (v_{cc}) and the lowest wordline voltage under which the write is possible when both bitlines are pre-charged [5]. The smaller the write margin the more difficult it is to write into an SRAM cell. Thus it is very difficult to optimize both the read and write margins at the same time. These margins will all degrade with the advent of scaling.

1.2 Research Objective

With current trends in CMOS technology and SRAM characterization, it is foreseeable that with extensive application of SRAM memories, read and write margins are degraded with scaling of CMOS thus alternative SRAM cells are required to achieve enhanced energy efficiency with scaling of power supply voltage. Under this context, this research investigation aims to investigate SRAM design trade-offs and develop guidelines for SRAM cell layout in 7nm FinFET technology.

1.3 Experimental Procedure

Initial data collection focused on supply voltage modulation at fixed temperature. Then Monte-Carlo trials are added at each supply voltage where statistical parameters are calculated. Using these statistics, empirical models are develop to account for read and write margin changes due to supply voltage modulation. A minimum supply voltage is then extracted from the margins using a linear least square regression. Finally, the v_t fluctuations are then analyzed to develop more insight into this pressing problem for nanoscale FinFET.

1.4 Supply Voltage Modulation

The data displayed below are those obtained by performing a DC sweep on Node 2/D to obtain the transfer characteristics of the MOSFET from $v_{cc} \in [0.18, 0.80]$ V. Fig. 1.4 and Fig 1.5 confirm the well-known trend that the read and hold margins are proportional to the supply voltage [6]. The butterfly curves get progressively smaller in terms of the area enclosed as the supply voltage decreases.

The write voltage margin is seen to have properties of a piecewise linear function. The majority of the data can be modelled by a best linear regression starting from about 0.3V and higher. Below 0.3V, a plateau has been reached. This indicates that the write margin has saturated where the difficulty in writing to a cell's logical state has reached a maximum. 0.3V can be considered to be the minimum supply voltage for the write margin. (More analysis will be shown in sec. 2.0 and 3.0)

Fig. 1.4) HSNM

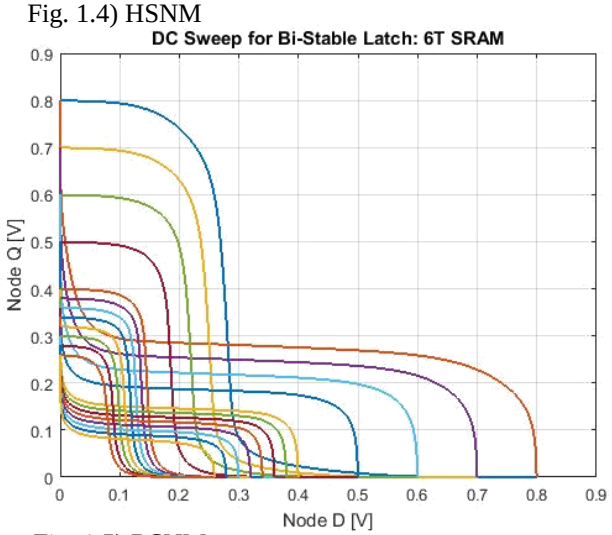


Fig. 1.5) RSNM

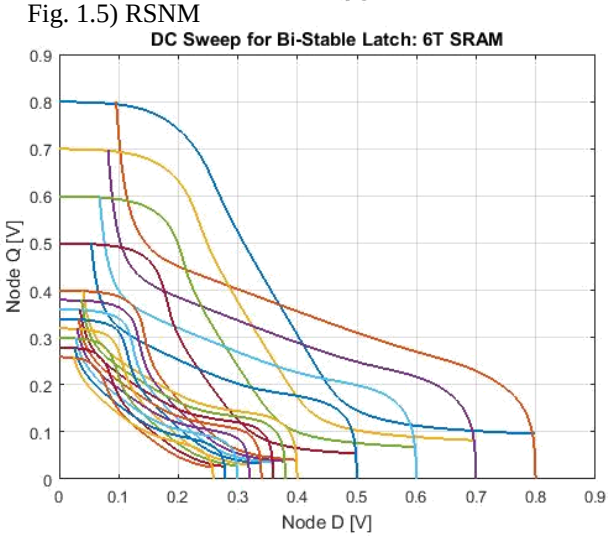
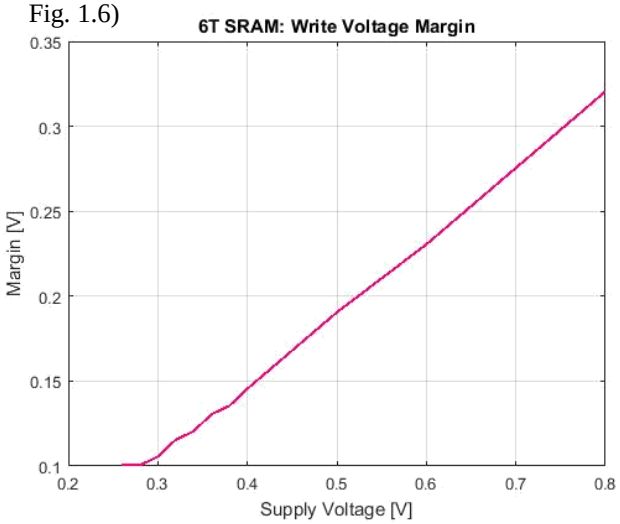


Fig. 1.6)



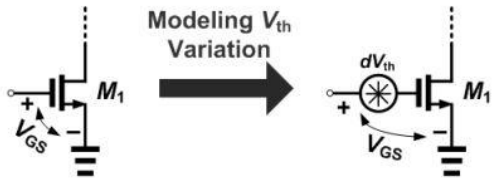
2.0 Monte Carlo Simulation: Theoretical Background

Monte Carlo method is a computer algorithmic approach to solving problems that are deterministic in principle with the idea of randomness [7]. It relies on draws from a prescribed probability distribution and performs a deterministic computation on these draws. In the context of this research investigation, Monte Carlo simulations are performed to model changes in threshold voltage—which forms a Gaussian distribution with a zero mean—due to process variation that occurs with the scaling of FinFET technology at 7nm.

2.1 Implementation in HSPICE

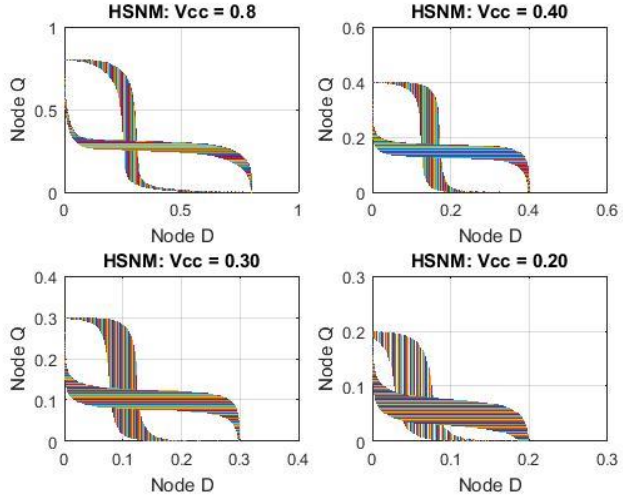
Actual implementations of Monte Carlo method is done in HSPICE simulation software for the 6T-SRAM cell designed. Before diving into experimental results, it is important to understand the background of the simulation done in HSPICE. To model changes in threshold voltage dv_{th} HSPICE uses a DC voltage source (see Fig. 1) connected between gate and ground for each FinFET used. This allows the user to set a particular distribution for dv_{th}. In sec. 2.0 and sec. 3.0, the absolute variation will be fixed at 50mV for a sigma value of 3.0. The standard deviation of the trials will then be on 6.67mV. More details of the distribution will be discussed in sec. 4.0.

Fig. 2.1) HSPICE Physical Model



Once the Gaussian distribution is set, the next step is to sample this distribution. This means that the Monte Carlo algorithm will random assign each of the transistors in the 6T-SRAM module a particular value of threshold voltage from the Gaussian distribution. The user is then required to input the number of samples drawn—the second most important parameter after selecting the probability density function. In this experiment, the number of samples N = 100 which gives a 95.2% CI [7]. This is a practical choice since normal semiconductor simulations would require 10,000 or more trials that would consume more time and computational resources [7].

Fig. 2.2) HSNM Monte Carlo Raw Data



2.2 Hold SNM: Monte Carlo Results

In MATLAB processing that followed, each Monte Carlo trial's threshold voltage combination and average, minimum, and standard deviation are being recorded for the given supply voltage value swept. The supply voltage sweep range is set to be $v_{cc} \in [0.18, 0.80]$ V.

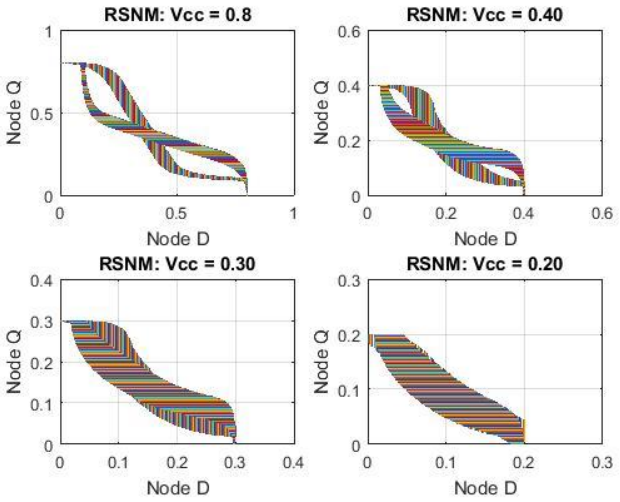
With the entirety of this background setting, a sample result has been displayed for the HSNM data at selected v_{cc} values. From Fig. 2.2, one can definitely witness shrinking of static noise margin or tolerance range as the supply voltage gets increasingly smaller. The group of ribbon stripes shown are from the DC voltage sweep of Node 2 (see section 1.0 for naming conventions) in the bi-stable latch structure of the SRAM module where each stripe corresponds to a particular selection/ draw of threshold voltage values from the PDF chosen in the Monte Carlo simulation at that trial.

2.3 Read SNM: Monte Carlo Results

Using similar procedures, the same experiment is now being run on 6T-SRAM with the access transistors turned on by the word-line voltage (WLV).

The results tell us that for $v_{cc} < 0.3$V the SRAM is no longer usable for read operation therefore establishing the fact that the minimum supply voltage for RSNM at 6.67 mV v_t standard deviation is approximately 0.3V. The exact same tests will later be repeated at different threshold variations to comprehensively account for threshold voltage influences (see section 4.0 for more details).

Fig. 2.3) RSNM Monte Carlo Raw Data



2.4 MATLAB Statistical Processing: SNM and WVM Data

To better understand the Monte Carlo-produced results, the average, standard deviation, and the minimum values for the SNM and WVM have been acquired at each v_{cc} value swept. The graphs below showcase the average hold and read SNM with the error bars representing the standard deviation calculated.

Fig. 2.4)

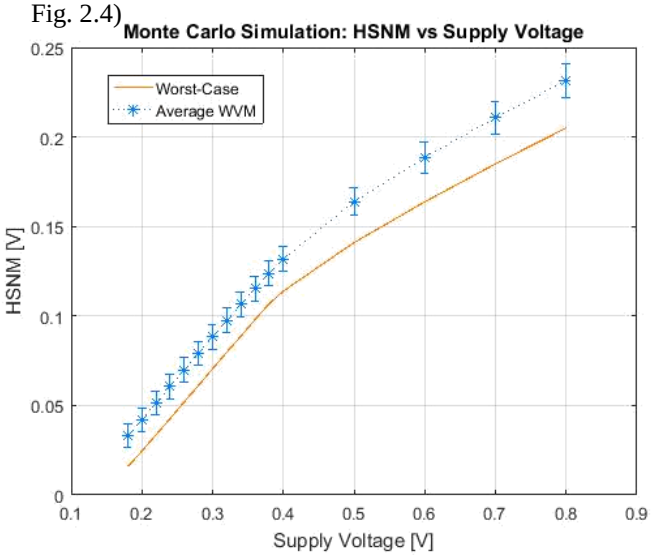
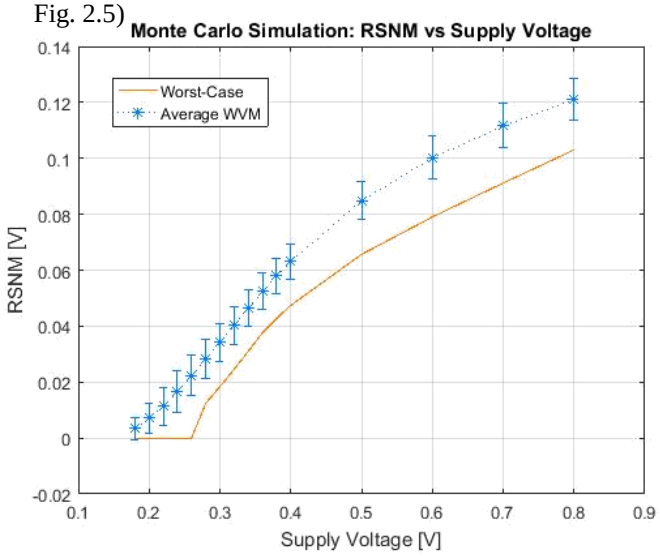


Fig. 2.5)



The orange-colored lines represent the minimum or worst-case SNM. It is these data that will be of crucial significance in determining the minimum supply voltage since the SRAM ceases normal operation when the worst-case SNM is lower than a tolerable threshold (here consider it to be zero). Fig. 2.6 below gives a direct comparison between the HSNM and RSNM worst-case values.

Fig. 2.6)

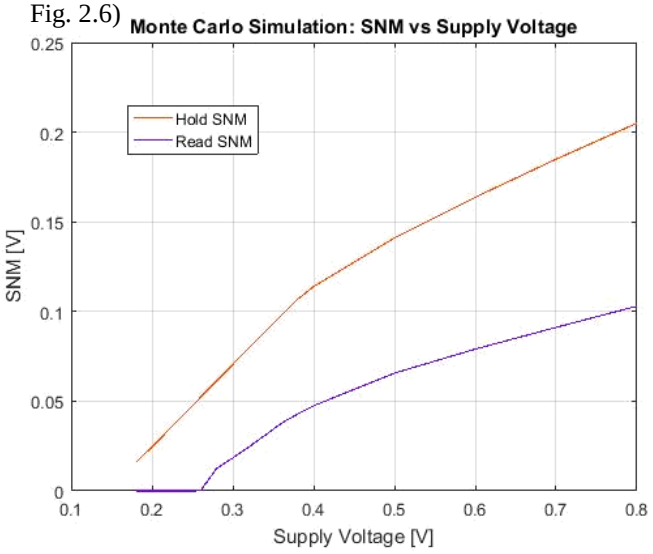
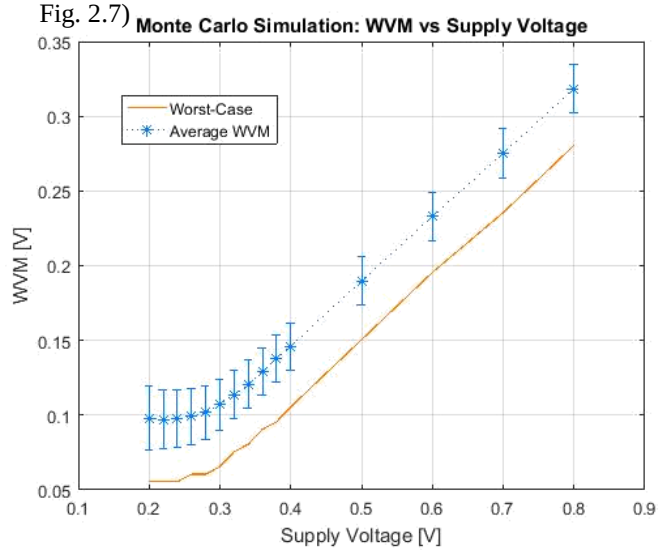


Fig. 2.7)



The results from Fig. 2.6 confirm the usual sense that HSNM > RSNM. The minimum supply voltage for HSNM will occur after RSNM's minimum supply voltage. Since minimum supply voltage is defined as the point where SNM or WVM becomes zero, graphs displayed in sections 3.0 and 4.0 are lower bound estimates. In reality, minimum supply voltage occurs at a point where the tolerance breaches below a certain threshold, usually 20mV in the practical cases. However, this is a systematic effect where an offset can be easily applied to adjust the threshold so to maintain consistency.

Additionally, to acquire minimum supply voltage a linear fit is used on the lower-v_{cc} portion of the data. Detailed extrapolation procedures are given in section 3.0.

2.5 Write Voltage Margin Data: Observations

Finally, the write voltage margin data is different from the SNM data based on the observed linearity throughout the testing domain. The worst-case curve experiences a plateau effect at lower supply voltages indicating termination in usable SRAM applications. Its minimum supply voltages will be also be lower bound estimates, though it gets more accurate at higher v_t variation levels (as seen in sec. 4.0).

3.0 SNM Trend Analysis: Nonlinear Least Square Regression

Given the data presented in the previous section, the following content addresses the problem of minimum supply voltage where the SRAM will experience ineffective SNM, and WVM (i.e. where SNM and WVM both become zero). Here all 100-Monte Carlo simulations was done at $\sigma(v_{th}) = \frac{50mV}{3} = 16.7mV$ such that the absolute variation was set at 50mV. Using this setup, a two-phase regression is observed in the SNM versus supply voltage trends. In order to numerically analyze the data, the form of regression defined by

$$\text{snm} = \alpha(\text{v}_{\text{cc}} - \text{v}_0)^{\beta} + \frac{\text{c}(\text{v}_{\text{cc}} - \text{v}_0)^{\delta}}{\exp(\varepsilon \text{v}_{\text{cc}})} \quad (1)$$

was used to model the SNM trends. This first component is used to model the power-function like growth at higher supply voltages. The second component describes the apparent linearity at lower supply voltages just before cutoff occurs. The key parameter in this model is v_0 that describes the cutoff/ minimum supply voltage. Using MATLAB's nonlinear custom "fittype" function, the above function was defined and matched using least square methods until a best match in coefficients occurs.

Fig. 3.1)

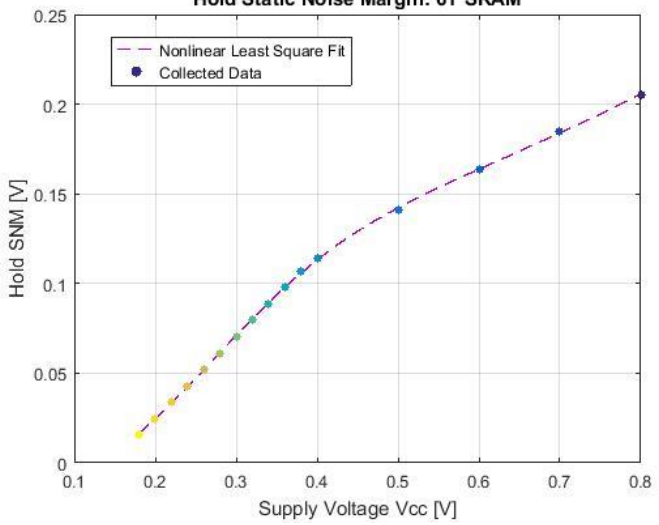


Fig. 3.2)

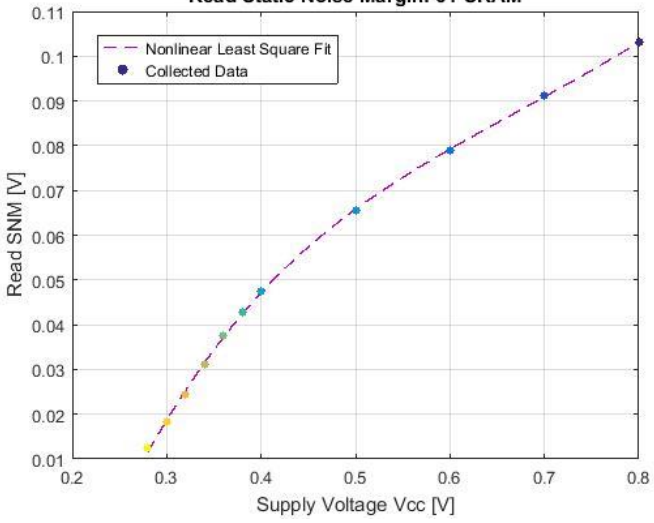


Table 3.1 **HSNM** Nonlinear Fit Coefficients

Variable	Average	95% CI Bounds	
α	0.2642	-0.1611	0.6895
β	5.2290	-1.6220	12.080
c	1.2770	0.6056	1.9490
δ	1.2520	1.1090	1.3950
ε	1.8120	0.9494	2.6750
v_0	**0.1452**	**0.1431**	**0.1472**

Table 3.2 **RSNM** Nonlinear Fit Coefficients

Variable	Average	95% CI Bounds	
α	0.1699	0.1249	0.2150
β	1.6970	-2.7100	6.1040
c	1.2850	-0.08718	2.6580
δ	1.1000	0.9803	1.2190
ε	3.4880	-2.3000	9.2750
v_0	**0.2479**	**0.2359**	**0.2599**

The theoretical minimum supply voltage is found to be +0.1452V and +0.2479V for H/R SNMs. Their 95% confidence interval (CI) bounds are given in the tables. In general, the minimum supply voltage should increase as $\sigma(v_{th})$ the standard deviation of the threshold voltage increases (explored in later sections).

3.1 WVM Trend Analysis: Linear Least Square Regression

Using both Monte Carlo analysis, and simple DC voltage sweep without accounting for threshold voltage variation, there is general linearity to be explored within the data points of the write voltage margin (WVM). As such, a linear regression was applied to the minimum write voltage margin values obtained using 100-Monte Carlo simulations at a standard deviation of $\sigma(v_{th}) = \frac{50mV}{3} = 16.7mV$. Thus the model is

$$\text{wvm} = \rho(\text{v}_{\text{cc}} - \text{v}_0) \quad (2)$$

Where ρ the slope of linear fit, and v0 is the minimum supply voltage of the write voltage margin.

Fig. 1.3)

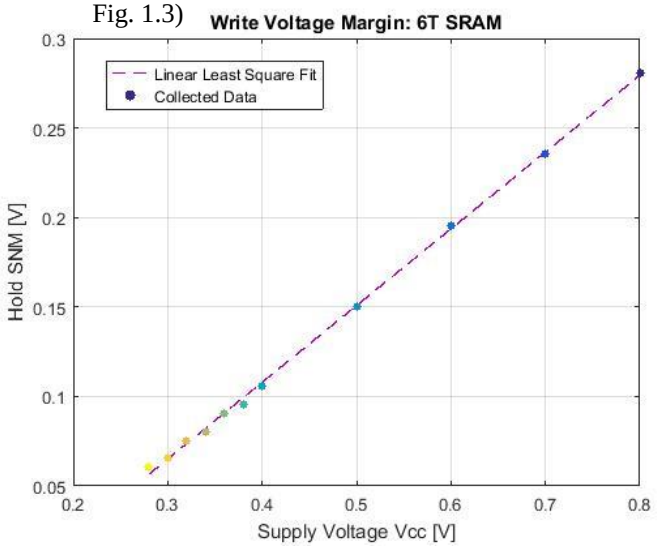


Table 3.3 WVM Linear Fit Coefficients

Variable	Average	95% CI Bounds	
ρ	0.4287	0.4191	0.4382
v_0	**0.1483**	**0.1405**	**0.156**

In the given case, the minimum supply voltage is extrapolated to be +0.1483V associated with a 95% confidence interval range.

It will be later shown that linear regression maintains a very good approximation to the WVM trends observed at higher standard deviation values for threshold voltage.

3.2 Numerical Analysis: Detailed Description

The application of Eq. (1) has shown merit in closely approximating the trend observed. The resultant error is negligible. Similar comments apply to Eq. (2). It must be noted that although the power exponents β and δ are both greater than unity in the given case; in general, it is expected both $\beta, \delta < 1.0$ as will be shown later that a less-than-unity growth factor is more suitable. However, the model is designed for both scenarios including when the exponents are negative. It is important to realize that the first term in Eq. (1) $\alpha(v_{cc} - v_0)^{\beta}$ has more influence than its second term $\frac{c(v_{cc}-v_0)^{\delta}}{\exp(\varepsilon v_{cc})}$ since the exponential factor is designed to reduce the first phase when the second phase starts. This ensures that the limiting form of the Eq. (1) becomes

$$\lim_{v_{cc}\to\infty} \alpha(v_{cc} - v_0)^{\beta} + \frac{c(v_{cc} - v_0)^{\delta}}{\exp(\varepsilon v_{cc})} = \alpha(v_{cc} - v_0)^{\beta} \qquad (3)$$

$$\therefore \mathbf{snm_{limit}} = \boldsymbol{\alpha}(\mathbf{v_{cc}} - \mathbf{v_0})^{\boldsymbol{\beta}} \qquad \text{for } v_{cc} > 0.5 \qquad (4)$$

In addition, like for the WVM, the static noise margin maintains this generic empirical trend under different standard deviation values for the threshold voltage (shown in sec. 4.0).

3.3 MATLAB Code Breakdown

As mentioned before, the MATLAB "fittype" and "fit" function was used to acquire the exact numerical fit. It is pertinent to consider the overall analysis procedure before proceeding onto the threshold voltage variation section. Here, the cutoff voltage was first estimated using the linear phase of the worst-case read SNM, solved as a "coefficient" type parameter with a 95% CI. The v_0 value was then passed as the value to a "problem" type parameter into the subsequent nonlinear fit. The format was chosen since MATLAB cannot pre-determine roots without resorting to complex analysis; this led to a two-step procedure as shown below:

Figure 3.4 MATLAB Code Segment: Regression Analysis

```
%Acquiring the cutoff voltage
[xr, yr] = prepareCurveData(Vcc, MinReadSNM);
xr = xr(5:length(xr),1);
yr = yr(5:length(yr),1);
fnc_root = fittype(@(c1, c2, x) c1*(x-c2), 'coefficients',{'c1','c2'});
f1 = fit(xr, yr, fnc_root);
%Re-establishing overall model with the obtained cutoff voltage
[x, y] = prepareCurveData(Vcc, MinReadSNM);
fnc_hsnm = fittype(@(a1, a2, a3, a4, a5, v0, x) a1*((x-v0).^a2)+a3*(((x-v0).^a4)./exp(a5*x))
f2 = fit(x, y, fnc_hsnm, 'problem', f1.c2);
```

Similar, analysis techniques will also be used for threshold voltage variation where instead of 2-Dimensional regression, a 3-Dimensional surface fit will be employed to model the multiple independent variables.

4.0 Threshold Voltage Variation Analysis

After Monte Carlo simulations are performed at a particular threshold voltage v_t variation level, the next step in the investigation of SRAM performance is to understand its behavior at multiple levels of v_t fluctuations. To begin, v_t variation is defined as the standard deviation of the threshold voltage $\sigma(v_t)$ in a Gaussian distribution. In HSPICE simulation, only an absolute variation can be specified at a particular sigma level such that the standard deviation is set to be the quotient of the two. In this experiment, sigma is set to 3.0. Thus the absolute variation is three times that of the standard deviation.

The range of variation is chosen to be $\sigma(v_t) \in [6.67, 50.0]$ mV. Remember, the absolute variation will then be 3 times that from $[20.0, 150.0]$ mV. Absolute variation will be used in all relevant figures. The Monte Carlo simulations performed in section 2.0 was set at $3\sigma(v_t) = 50.0$ mV; now HSPICE will repeat similar data collection but at multiple $\sigma(v_t)$ data points. This allows us to plot the minimum supply voltages as a function of different $3\sigma(v_t)$ levels:

Fig. 4.1)

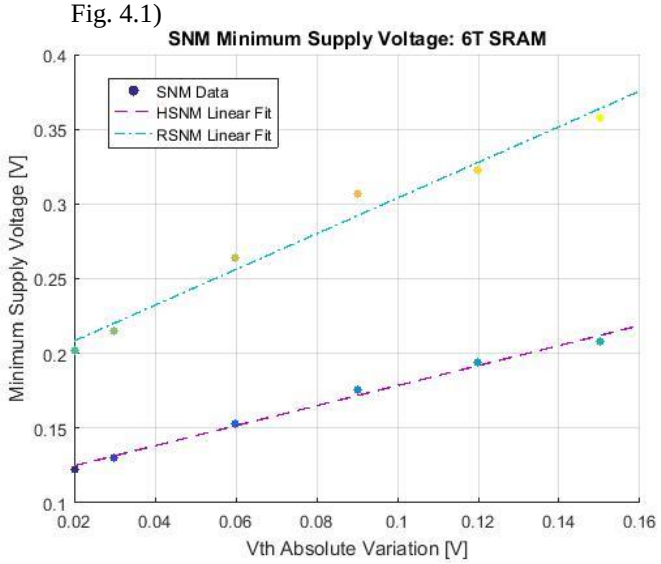
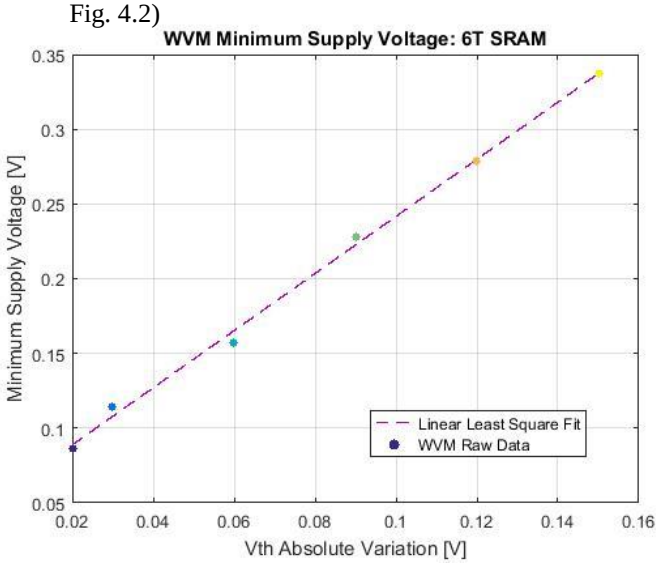


Fig. 4.2)



Based on the data collected above, observe that minimum supply voltage v_0 exhibits a high degree of linearity with respect to absolute variation of v_t. Linear regressions are then applied to both SNM and WVM raw data. Let absolute variation $\chi = 3\sigma(v_t)$ then

$$v_o(\chi) = c_1\chi + c_2 \tag{5}$$

Using MATLAB fit and fittype functions the following regression fit tables are generated:

Table 4.1 HSNM: Min Supply Voltage

Variable	Average	95% CI Bounds	
c_1	0.6706	0.5849	0.7563
c_2	0.1114	0.1036	0.1192

Table 4.2 RSNM: Min Supply Voltage

Variable	Average	95% CI Bounds	
c_1	1.194	0.9462	1.443
c_2	0.1845	0.1618	0.2071

Table 4.3 WVM: Min Supply Voltage

Variable	Average	95% CI Bounds	
c_1	1.911	1.767	2.055
c_2	0.05059	0.03748	0.06371

Note: Table 4.3 will later be compared with an extracted min supply voltage curve from a planar fit of WVM data accounting for threshold voltage variations.

4.1 Static Noise Margin: Empirical Formulation and Analysis Procedure

To analyze the threshold variation data, the approach taken in this section mirrors and further extends the approach used in Sec 3.0 and beyond. In section 3.0, a 2-phase empirical formula found great success in describing the trends observed in static noise margin data. This allowed the following curve to be implemented:

$$f(v_{cc}) = \alpha(v_{cc} - v_0)^{\beta} + \frac{c(v_{cc} - v_0)^{\delta}}{\exp(\varepsilon v_{cc})} \tag{6}$$

Continuing on this basis, in general, it can be postulated the static noise margin is a function of both v_{cc} and v_0, but its internal composition demands more analysis.

Using a partially-separable function allows fluctuations in static noise margin to be estimated with a high degree of accuracy. This extended empirical formula builds upon the previous single variable version used at a fixed threshold variation level. It takes on the following form

$$T(v_{cc},\chi) = \frac{\alpha}{v_0(\chi)} f(v_{cc},\chi) \tag{7}$$

$$T(v_{cc},\chi) = \frac{\alpha}{v_0(\chi)}\left[(v_{cc}-v_0(\chi))^{\beta} + \frac{c'(v_{cc}-v_0(\chi))^{\delta}}{\exp(\varepsilon v_{cc})}\right] \tag{8}$$

Based on data observations, $v_0(\chi)$ is in general a linear function of χ so this means that the final form of the static noise margin $T(v_{cc},\chi)$ will become:

$$\therefore T(v_{cc},\chi) = \alpha v_0(\chi)^{-1}\{[v_{cc}-(c_1\chi+c_2)]^{\beta} + c'\exp(-\varepsilon v_{cc})[v_{cc}-(c_1\chi+c_2)]^{\delta}\} \tag{9}$$

The reason for including $v_0(\chi)^{-1}$ will shortly be explained.

4.2 Hold Static Noise Margin: Surface Fit and Error Contour

Using the empirical model, surface fit and error contour are being simulated and graphed in MATLAB. This yielded the following results:

Fig. 4.3)

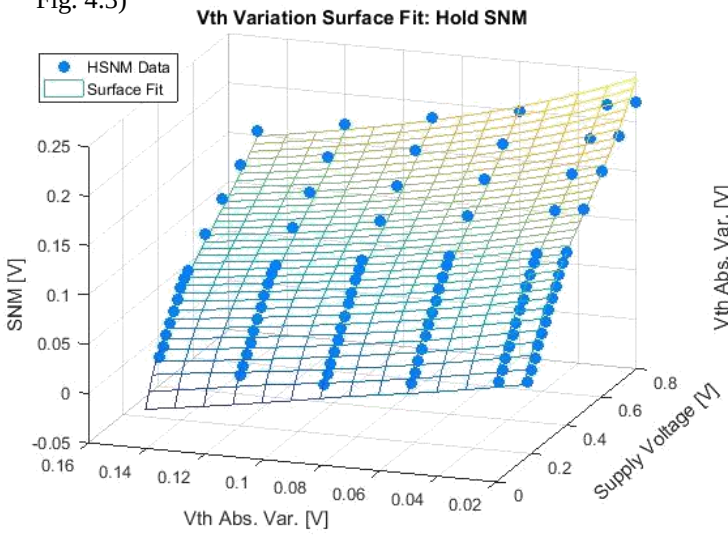


Fig. 4.4)

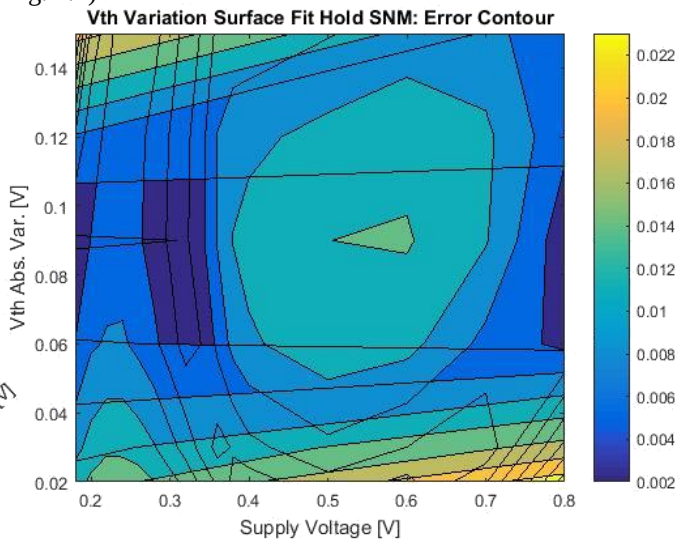


Table 4.4 HSNM Surface Fit

Variable	Average	95% CI Bounds	
α	+4.022	-339.20	+347.3
β	+1.268	+0.6038	+1.931
c	-4.100	-347.20	+339.0
δ	+1.289	+0.1068	+2.471
ε	+0.02928	-2.4910	+2.550

Table 4.5 RSNM Surface Fit

Variable	Average	95% CI Bounds	
α	0.08462	0.005679	+0.1636
β	+1.034	+0.7458	+1.322
c	-1.030	-5.6370	+3.577
δ	+2.915	-0.02683	+5.858
ε	+2.790	-2.8480	+8.429

Note: Surface regression and error contour for RSNM are found in next section.

Fig. 4.3 and 4.4 reveals that the error of the empirical function is constrained around 3.0% ~ 4.0%. This shows that the chosen $T(v_{cc},\chi)$ model is well designed. Overall from Fig. 4.4, the error contour confirms the theoretically predicted trend that as the supply voltage scales to smaller extent and with the increase in threshold variation, the degree of uncertainty becomes higher. This causes the error rate to be approximately 20mV in static noise margin, a significant increase. The contour guarantees an error of less than 10mV as long as the threshold absolute variation is less than 0.l V. Moreover, it is important to note that the second phase inherit to the HSNM data has a β-parameter being greater than unity (β = 1.268 > 1.0), deviating from the previous power-like growth as observed in section 2.

The resultant model $T(v_{cc},\chi)$ includes $v_0(\chi)^{-1}$ in front of $f(v_{cc},\chi)$ in order to introduce a relative weighting factor among different χ-levels tested from systematic uncertainties. In a more general case, polynomial weighting function can also serve the model where the weighting function $w(\chi)$ becomes:

$$w(\chi) = \sum_{i=0}^{n} p_i\chi^i \Rightarrow T_{general}(v_{cc},\chi) = w(\chi)\left[(v_{cc}-v_0(\chi))^{\beta} + \frac{c'(v_{cc}-v_0(\chi))^{\delta}}{\exp(\varepsilon v_{cc})}\right] \tag{10}$$

In $T_{general}(v_{cc}, \chi)$, $v_0(\chi)$ would still remain to be the form obtained from the minimum supply voltage versus threshold variation data. Weighting $w(\chi)$ can be adjusted as needed in order to reduce the uncertainty. The reason for letting $w(\chi) = \alpha \cdot v_0(\chi)^{-1}$ is due to the nature of the x-y plane intercept function which reveals an inverse relationship between the threshold variation and the supply voltage.

4.3 Read Static Noise Margin: Surface Fit and Error Contour

Applying similar models to the read SNM, with the same form of $v_0(\chi)$ and letting $w(\chi) = \alpha \cdot v_0(\chi)^{-1}$, the following graphs for RSNM are generated:

Fig. 4.5)

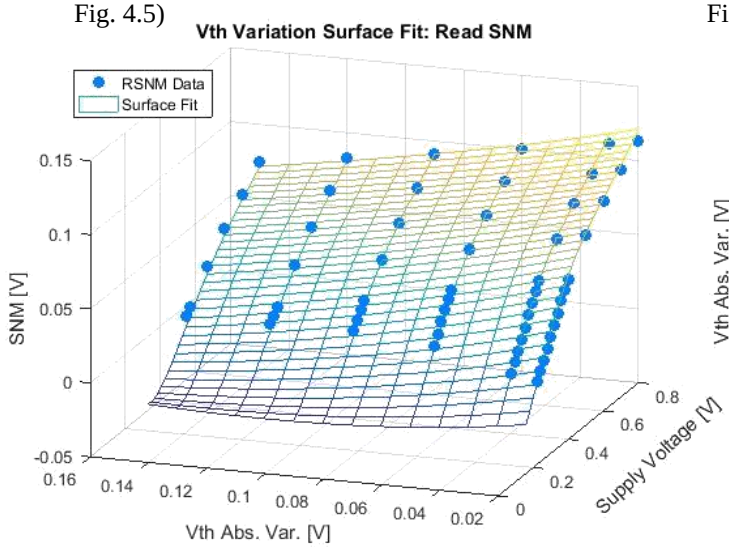
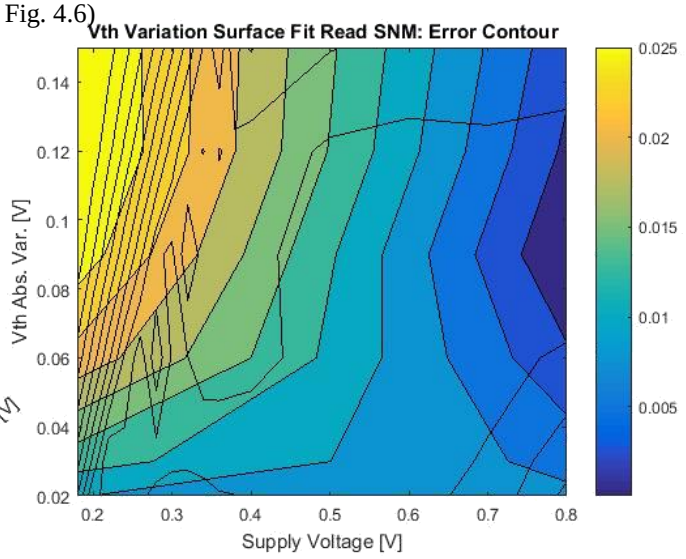


Fig. 4.6)



RSNM threshold voltage variation exhibited a higher degree of fluctuation than HSNM as expected from the degradation of the read margin due to the activation of the access transistors. The error contour displays a much clearer trend than the Fig. 4.4 above. The lowest uncertainty results from higher supply voltage and lower absolute variation. Progressing steadily toward lower supply voltage and higher threshold variation, the errors become increasingly noticeable as from the change in the spatial contour fillings.

4.4 Write Voltage Margin: Planar Fit and Extracted $v_0(\chi)$ Curve

To analyze the write voltage margin, the approach taken is somewhat different from that of static noise margin. The high degree of linearity presented in the WVM data allows us to consider a planar fit toward the resultant surface. This planar surface is defined as follows:

$$T_{wvm}(v_{cc}, \chi) = av_{cc} + b\chi + c \tag{11}$$

Instead of an error contour, an extracted $v_0(\chi)$ curve from the equation $T_{wvm}(v_{cc}, \chi) = 0$ is used to measure the relative error of the surface fit. Theoretically, if all was a perfect match then

$$v_0(\chi)_{estimate} = -\frac{b}{a}\chi - \frac{c}{a} \cong c_1\chi + c_2 \tag{12}$$

Based on this method, the following graphs result:

Fig. 4.7)

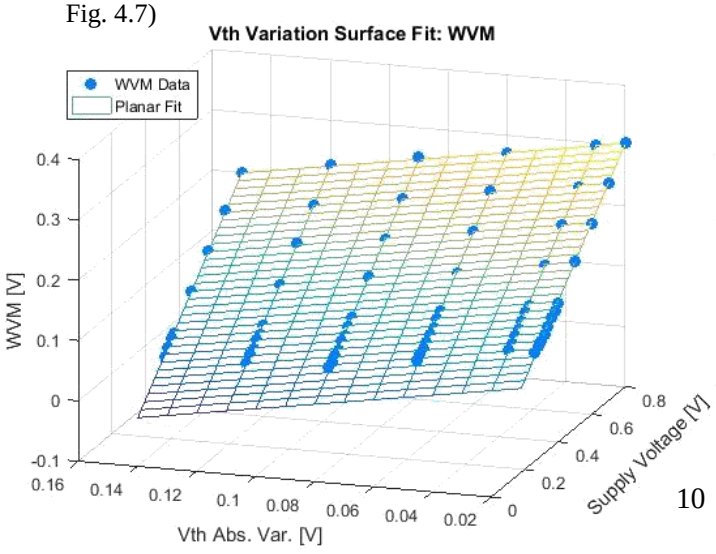


Fig. 4.8)

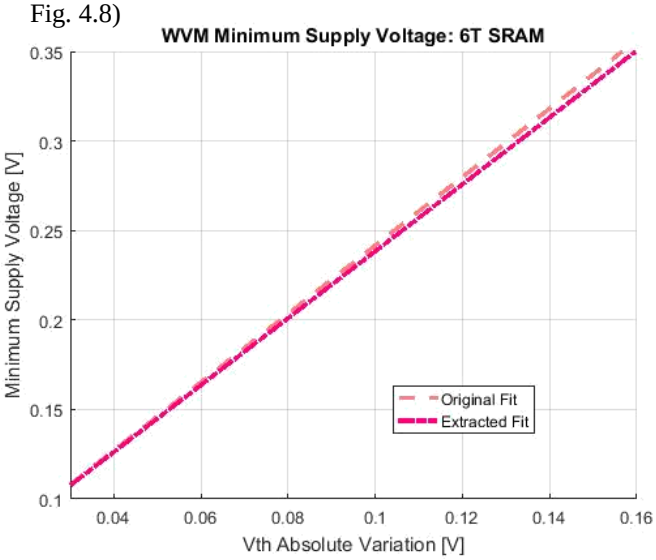


Table 4.6 WVM Planar Fit

Variable	Average	95% CI Bounds	
a	+4.022	-339.20	+347.3
b	+1.268	+0.6038	+1.931
c	-4.100	-347.20	+339.0

Table 4.7 Extracted $v_0(\chi)_{estimate}$ Parameters

Variable	Average	95% CI Bounds	
c_1	0.08462	0.005679	+0.1636
c_2	+1.034	+0.7458	+1.322

Note: Table 7 is plotted in Fig. 8) above.

From Fig. 4.7 the obtained WVM – v_t variation data is seen to follow a planar fit defined above with little fluctuations from the generic trend. Later processing revealed the maximum error is less than 4.0% of the actual data value, indicating a well-designed empirical model.

Moreover, the extracted $v_0(\chi)_{estimate}$ curve was then plotted in Fig. 4.8 and compared to the original minimum supply voltage versus χ curve, $v_0(\chi)$, where the two curves are seen to have little deviation over the testing range of $3\sigma(v_t)$, the absolute variation of the threshold voltage. This again implies that the model and the raw data highly correlates to each other.

4.5 MATLAB Code Breakdown

To analyze the SNM and WVM raw data, MATLAB processing was key in uncovering the details described above as well as generating the graphs displayed. This section briefs the programming which led to the results for the benefit of future works in the same field of investigation.

The initial phase was to extract the minimum supply voltage acquired from section 3.0 but for each χ-level tested. Similarly, the processed average and worst-case SNM and WVM values from section 2.0 are first written into excel and re-organized before acquiring into section 4.0's MATLAB code. Under this context, the processing begins by formulating $v_0(\chi)$ curve that was displayed in Table 1 – 3.

Fig. 9) $v_0(\chi)$-Regression Code

```
%% Acquiring the cutoff voltage vs vth var. curve - using linear fitting
[x, y] = prepareCurveData(AbsVar_prime, v0);
fnc_L1 = fittype(@(a, b, x) a*x+b, 'coefficients',{'a','b'});
L1 = fit(x, y, fnc_L1);
```

Note this is different from section 3.0 where similar code was used to acquire the minimum supply voltage, but here the programming aims to establish a linear model between v_0 and χ.
The surface fit used fit and fittype functions defined previously in section 3.0.

Fig. 10) SNM – Surface Fit Code

```
%% Surface Regression Fit: SNM Values
surf_HSNM = fittype('(1./(c1*y + c2))*(a1*((x-(c1*y + c2)).^a2)+a3*(((x-(c1*y + c2)).^a4)./exp(a5*x)
[X, Y, Z] = prepareSurfaceData(Vcc, AbsVar, MinSNM);
S1 = fit([X,Y],Z,surf_HSNM,'problem',{L1.a, L1.b});
```

The most difficult part of the graphics to acquire was the error contour. The error contour required an appropriately sized mesh in the x-y plane to be first established before any processing can be done. With the mesh grid comes the question of acquiring the necessary raw data from excel. It is important to note that due to the error contour setup, some deviant data points that would otherwise be removed was also incorporated into the error contour. They showed slight effect in HSNM plotting in Fig. 4) at the lower right-hand corner.

Fig. 11) SNM – Error Contour Code

```
for row = 1:num
    for col = 1:num
        Vcc_req = X_contour(row,col);   % Acquire Vcc and AbsVar we are testing
        AbsVar_req = Y_contour(row,col);
        [matrix_row, r_index] = find(test_Vcc == Vcc_req);  % Acquire the relative index in the cell array
        [cell_row, r_index] = find(test_AbsVar == AbsVar_req);
        % Acquire the actual data in the cell array for the SNM mesh
        SNM_actual(row,col) = contourData{cell_row,1}(matrix_row,1);
    end
end
Z_contour = (1./((L1.a).*Y_contour + L1.b)).*( (S1.a1)*(X_contour - ((L1.a).*Y_contour + L1.b)).^(S1.a2) +
Z_contour = real(Z_contour); % computing the predicted values
ErrorSNM = abs(SNM_actual - Z_contour); % Error = Abs(Actual - Predicted)
figure; v_level = 0.002:0.003:0.0250;
[C, h] = contourf(X_contour, Y_contour, ErrorSNM, v_level); colorbar; % plotting the contour
```

To assist the reader in exploring numerical values, a colorbar was included to aid in the visual details. This is shown in both Fig. 4 and Fig. 6.

5.0 Conclusion and Future Work Recommendation

The results of this project has solidified several key observations. Firstly, the supply voltage modulation causes a two-phase static noise margin in both standby and read scenarios. This is modelled using Eq. (1). The write voltage margin was observed to behave in linear-fashion in both supply voltage modulation and threshold voltage variation which eventually let $T_{wvm}(v_{cc}, \chi)$ define a least square plane fit. The error contours all confirm that more significant uncertainties occur at high threshold fluctuation and low supply voltage in static noise margin. The write margin has a general-low error model as seen in Fig. 4.8) from the extracted $v_0(\chi)_{estimate}$ curve that was later compared to the original $v_0(\chi)$ curve obtained from the raw v_0 values.

It is important to note that the weighting function is set to $w(\chi) = \alpha v_0(\chi)^{-1}$ where $v_0(\chi)^{-1}$, reciprocal of minimum supply voltage. This can be further expanded into a polynomial within the χ-space as described in Eq. (10) where degree n is chosen to achieve a particular yield. In addition, the weighting function can be turned into a multiple-variable accounting for other variables as well where $w = w(\chi, v_{cc}, \dots)$ as an example. Essentially, the choice of the weighting function is determined by the nature of the problem and the level of precision required.

The choice of the number of Monte Carlo trials is another parameter to be discussed. In the given experiment, an approximate 95.2% confidence interval was guaranteed using 100 trials per variation [7]. This number can be further increased if the CI rate was set higher. N = 100 was selected due to its relative short time span needed to complete the simulation and the less computational resources spent. For future projects, it is recommended to have at least 10,000 trials for better results, though the given experiment's CI rate was sufficient to draw clear conclusions from.

It was mentioned in previous sections that the minimum supply voltage was acquired using a linear regression on the lower part of the data where linearity was exhibited. This made the point where the static noise margin and the write margin both became zero the point of minimum supply voltage. This can be a serious underestimation for lower $\sigma(v_t)$ but as $\sigma(v_t)$ increases this underestimation reduces. Fortunately, this is a systematic error that can be corrected but pre-setting a target voltage below which can be said the SRAM is rendered unusable.

With the results of this experimentation, it is advised that future investigations relating to this area focus on alternative SRAM cell designs such as the 7T, 8T, and 9T SRAM cells by repeating the analysis done here with necessary modifications so that a more comprehensive scope is covered to better develop SRAM design guidelines and learn more about device characterizations.

6.0 Acknowledgements

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